IN THE CLAIMS:

Please cancel claims 20, 22-27, 29-34 and 36-40 with ut prejudice to or disclaimer of the subject matter contained therein.

Please add the following new claims:

41. (Newly Added) A semiconductor integrated circuit device comprising:

a semiconductor substrate of a first conductivity type;

at least two first well regions of a second conductivity type formed in the semiconductor substrate;

at least one second well region of the first conductivity type formed in the at least two first well regions, and

semiconductor MOSFET elements formed in the at least two first well regions and the at least one second well region,

wherein a memory circuit comprises the semiconductor MOSFET elements.

42. (Newly Added) A semiconductor integrated circuit device comprising:

a semiconductor substrate of a first conductivity type;

at least two first well regions of a second conductivity type formed in the semiconductor substrate; and

integrated circuits which are formed on the at least two first well region respectively, and which have different functions.

43. (Newly Added) The semiconductor integrated circuit device according to claim 42, wherein a second well region of the first conductivity type is formed in at least one of the at least two first well regions, and one of the integrated circuits is formed on the at least one of the at least two first well regions and the second well region.

44. (Newly Added) The semiconductor integrated circuit device according to claim 42, wherein a second well region of the first conductivity type having a third well region of the second conductivity type formed therein is formed in at least one of the at least two first well regions, and one of the integrated circuits is formed in the at least one of the at least two first well regions, the second well region and the third well region.

45. (Newly Added) The semiconductor integrated circuit device according to claim 41, wherein a potential supplied to the at least tw first well regions differs from a potential supplied to the at least one second well region.

46. (Newly Added) The semiconductor integrated circuit device according to claim 42, wherein a potential is supplied to the at least two first well regions.

47. (Newly Added) The semiconductor integrated circuit device according to claim 43, wherein a potential supplied to the at least two first well regions differs from a potential supplied to the second well region.

48. (Newly Added) The semiconductor integrated circuit device according to claim 44, wherein a potential supplied to the at least two first well regions differs from a potential supplied to the second well region.

49. (Newly Added) The semiconductor integrated circuit device according to claim 42, wherein at least one of the integrated circuits is one of a non-volatile memory circuit, an analog circuit, a digital circuit, a digital/analog circuit, a static memory circuit, a random-access memory circuit, and a processor circuit.

50. (Newly Added) The semiconductor integrated circuit device according to claim 49, wherein each of the integrated circuits has a potential application terminal for receiving a different potential applied thereto.

51. (Newly Added) The semiconductor integrated circuit device according to claim 50, wherein each of the integrated circuits has a dedicated output terminal for outputting an output signal when the potential is applied to the potential application terminal thereof.

52. (Newly Added) The semiconductor integrated circuit device according to claim 51, wherein each of the integrated circuits includes a c ntrol circuit for performing on/off control of application of the potential to the potential application terminal thereof.

53. (Newly Added) The semiconductor integrated circuit device according to claim 52, wherein each of the integrated circuits includes a voltage generating circuit for application of the potential to the potential application terminal thereof.

54. (Newly Added) The semiconductor integrated circuit device according to claim 42, further comprising:

a bias wiring system for supplying a bias potential to the semiconductor substrate; and

a power supply wiring system for supplying operation power to the integrated circuits,

wherein the bias wiring system and the power supply wiring system are located such that the bias wiring system and the power supply wiring system are independent of and not connected to each other.

55. (Newly Added) The semiconductor integrated circuit device according to claim 44, wherein a back gate bias is supplied to the third well region, and an input/output circuit or an interface circuit is formed in the third well region and the second well region in which the third well region is formed.

56. (Newly Added) A test method of testing semiconductor integrated circuit devices each comprising a semiconductor substrate of a first conductivity type, at least two first well regions of a second conductivity type formed separately in the semiconductor substrate, integrated circuits formed on the at least two first well regions, respectively, and having different functions, potential application terminals included in the integrated circuits, respectively, each of which for receiving a different potential applied thereon, and dedicated output terminals provided in the integrated circuits, respectively, for outputting output signals, the method comprising:

for at least one of the semiconductor integrated circuit devices,

applying potentials to potential application terminals of at lest two of the integrated circuits simultaneously and in parallel;

detecting output data output respectively from dedicated output terminals of the at least two of the integrated circuits to which the potentials are applied;

determining whether the detected output data have a defect or not; and

shutting off application of a potential to a potential application terminal of an integrated circuit if output data therefrom is determined as having said defect.

57. (Newly Added) The test method according to claim 56, wherein

the integrated circuits include control circuits, respectively, for performing on/off control of application of potentials to the potential application terminals provided in the integrated circuits, and

application of the potential to the potential application terminal of the integrated circuit from which the output data having the defect is output is shut off by supplying a control signal to a control circuit of the integrated circuit from which the output data having the defect is output.

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58. (Newly Added) The test method according to claim 57, wherein

the integrated circuits include voltage generating circuits, respectively, for application of the potentials to the potential application terminals provided in the integrated circuits, and

application of the potential to the potential application terminal of the integrated circuit from which the output data having the defect is output is shut off by supplying a control signal from a voltage generation circuit of the integrated circuit from which the output data having the defect is output to the control circuit of the integrated circuit from which the output data having the defect is output.

59. (Newly Added) The test method according to claim 56, wherein

the output data output respectively from the dedicated output terminals of the at least two of the integrated circuits are potentials therein, and

whether the detected output data have a defect or not is determined by determining whether a variation in potential in each of the at least two of the integrated circuits falls within a predetermined range of allowance.

60. (Newly Added) The test method according to claim 56, wherein two or more of the integrated circuits are tested simultaneously and in parallel by the test method.

61. (Newly Added) The test method according to claim 59, wherein two or more of the integrated circuits are tested simultaneously and in parallel by the test method.

62. (Newly Added) A test device for testing semiconductor integrated circuit devices each comprising a semiconductor substrate of a first conductivity type, at least two first well regions of a second conductivity type formed separately in the semiconductor substrate, integrated circuits formed on the at least two first well regions, respectively, and having different functions, potential application terminals included in the integrated circuits, respectively, each of which for receiving a different potential applied thereon, and dedicated output terminals provided in the integrated circuits, respectively, for outputting output signals, the test device comprising:

for at least one of the semiconductor integrated circuit devices,

a power source for applying potentials to potential application terminals of at least two of the integrated circuits;

a detection circuit for detecting output data output from dedicated output terminals of the at least two of the integrated circuits to which the potentials are applied;

a judgment circuit for determining whether the detected output data have a defect; and

a shut-off circuit for shutting off application of a potential to a potential application terminal of an integrated circuit if output data therefrom is determined by the judgment circuit as having said defect.

63. (Newly Added) The test device according to claim 62, wherein

the integrated circuits include control circuits, respectively, for performing on/off control of application of potentials to potential application terminals provided in the integrated circuits, and

a control signal for shutting off application of the potential to the potential application terminal of the integrated circuit from which the output data having the defect is output is supplied to a control circuit of the integrated circuit from which the output data having the defect is output.